VND5E004A-E
VND5E004ASP30-E

Double 4mΩ high-side driver with analog current sense for automotive applications

Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 28 V
Max on-state resistance (per ch.)	R_{ON}	4 mΩ
Current limitation (typ)	I_{LIMH}	90 A
Off-state supply current	I_S	2 µA(1)

1. Typical value with all loads connected

- General
  - Very low standby current
  - 3.0 V CMOS compatible inputs
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - Compliant with European directive 2002/95/EC
  - Very low current sense leakage
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide currents range
  - Diagnostic enable pin
  - Off-state open-load detection
  - Output short to V_{CC} detection
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
- Protection
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Overtemperature shutdown with auto restart (thermal shutdown)
  - Inrush current active management by power limitation
  - Reverse battery protection with self switch on of the Power MOSFET
  - Electrostatic discharge protection



PQFN - 12x12 Power lead-less   MultiPowerSO-30

Applications

- All types of resistive, inductive and capacitive loads
- Suitable for power management applications

Description

The VND5E004A-E and VND5E004ASP30-E are double channel high-side drivers manufactured using ST proprietary VIPower™ M0-5 technology and housed in PQFN-12x12 power lead-less and MultiPowerSO-30 packages. The devices are designed to drive 12 V automotive grounded loads, and to provide protection and diagnostics. They also implement a 3 V and 5 V CMOS-compatible interface for use with any microcontroller.

The devices integrate advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto-restart and overvoltage active clamp. A dedicated analog current sense pin is associated with every output channel providing enhanced diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication, overtemperature indication, short-circuit to V_{CC} diagnosis and on-state and off-state open-load detection. The current sensing and diagnostic feedback of the whole device can be disabled by pulling the DE pin low to share the external sense resistor with similar devices.

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1 Block diagram and pin configurations

Figure 1. Block diagram

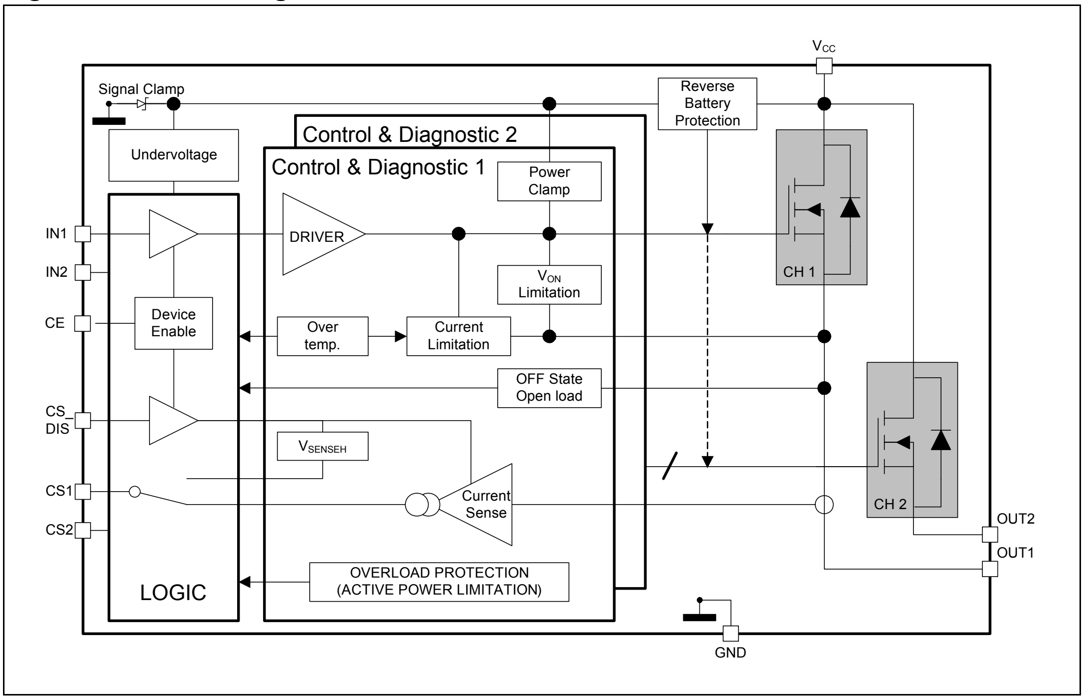


Table 1. Pin functions

Name	Function
V_{CC}	Battery connection
OUT1,2	Power output
GND	Ground connection
IN1,2	Voltage controlled input pin with hysteresis, CMOS compatible, controls output switch state
CS1,2	Analog current sense pin; delivers a current proportional to the load current
DE	Active high diagnostic enable pin

Figure 2. Configuration diagram (not in scale)

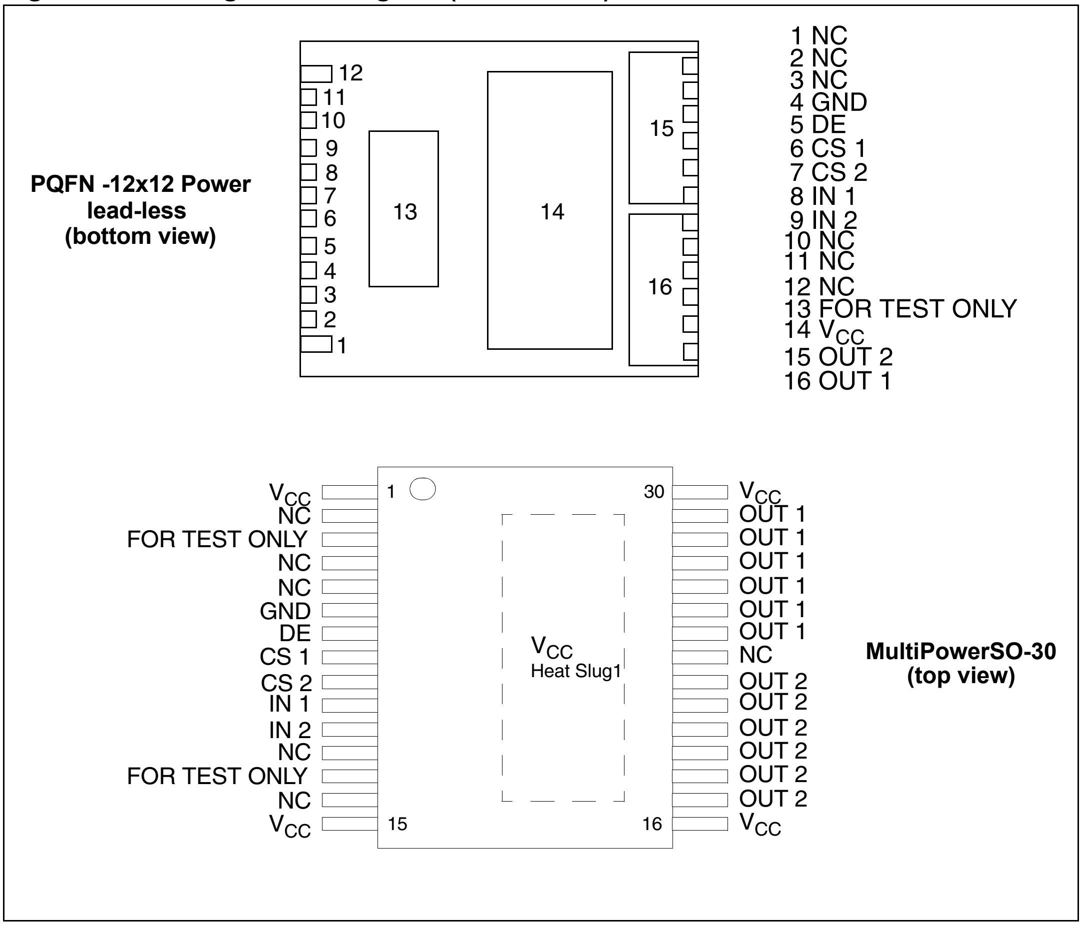


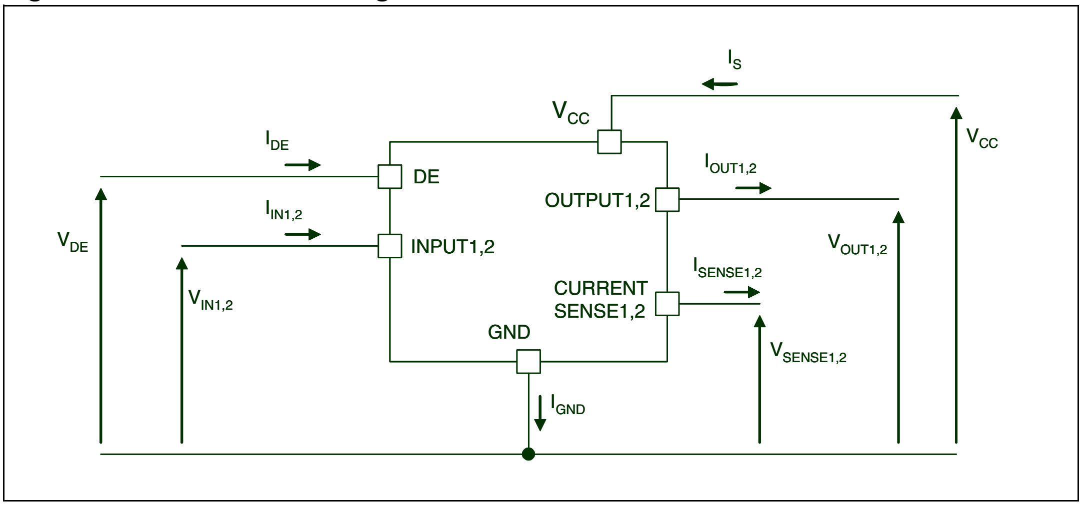
Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	NC(1)	Output	Input	DE	For test only
Floating	Not allowed	X	X	X	X	X
To ground	Through 1kΩ resistor	X	Not allowed	Through 10kΩ resistor	Through 10kΩ resistor	Not allowed

1. Not connected

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Applying stress which exceeds above the ratings listed in *Table 3: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	28	V
V_{CCPK}	Transient supply voltage ($T < 400$ ms, $R_{load} > 0.5\ \Omega$)	41	V
$-V_{CC}$	Reverse DC supply voltage	16	V
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	70	A
I_{IN}	DC input current	-1 to 10	mA
I_{DE}	DC diagnostic enable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage ($V_{CC} > 0$ V)	V_{CC}-41 $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) ($L = 0.3$ mH; $R_L = 0\ \Omega$; $V_{bat} = 13.5$ V; $T_{jstart} = 150$ °C; $I_{OUT} = I_{limL}$(Typ.))	600	mJ
V_{ESD}	Electrostatic discharge (Human Body Model: $R = 1.5\ k\Omega$; $C = 100$ pF)	2000	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Maximum value		Unit
		MultiPowerSO-30	12x12 PLLP	
$R_{thj\text{-}case}$	Thermal resistance junction-case (with one channel ON)	0.35	0.35	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	58(1)	39(2)	°C/W

1. PCB FR4 area 58 mm x 58 mm, PCB thickness 2 mm, Cu thickness 35 µm, minimum pad layout
2. PCB FR4 area 78 mm x 78 mm, PCB thickness 2 mm, Cu thickness 35 µm, minimum pad layout

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 24 V, -40 °C < T_j < 150 °C, unless otherwise stated.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance(1)	I_{OUT} = 15 A; T_j = 25 °C		3		mΩ
		I_{OUT} = 15 A; T_j = 150 °C			6	mΩ
		I_{OUT} = 15 A; V_{CC} = 5 V; T_j = 25 °C			6	mΩ
$R_{ON\ REV}$	R_{DSon} in reverse battery condition	V_{CC} = -13 V; I_{OUT} = -15 A; T_j = 25 °C		3		mΩ
V_{clamp}	V_{CC} clamp voltage	I_{CC} = 20 mA; $I_{OUT1,2}$ = 0 A	41	46	52	V
I_S	Supply current	Standby V_{DE} = 0 V; V_{CC} = 13 V; T_j = 25 °C; V_{IN} = 0; V_{OUT} = V_{SENSE} = 0 V		2	5	µA
		Off-state; V_{CC} = 13 V; V_{DE} = 5 V; T_j = 25 °C; V_{IN} = V_{OUT} = V_{SENSE} = 0 V		10	15	µA
		On-state; V_{CC} = 13 V; V_{DE} = 5 V; V_{IN} = 5 V; I_{OUT} = 0 A		3.5	6	mA
$I_{L(off)}$	Off-state output current (1)	V_{IN} = 0 V or V_{DE} = 0 V; V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25 °C	0	0.01	3	µA
		V_{IN} = 0 V or V_{DE} = 0 V; V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125 °C	0		5	µA

1. For each channel

Table 6. Switching (V_{CC} = 13 V; T_j = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 0.87 Ω (see *Table 6*)	—	25	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 0.87 Ω (see *Table 6*)	—	35	—	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 0.87 Ω	—	See *Figure 26*	—	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 0.87 Ω	—	See *Figure 28*	—	V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 0.87 Ω (see *Table 6*)	—	5.4	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 0.87 Ω (see *Table 6*)	—	2.3	—	mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL1,2}$	Input low level voltage				0.9	V
$I_{IL1,2}$	Low level input current	V_{IN} = 0.9 V	1			µA
$V_{IH1,2}$	Input high level voltage		2.1			V
$I_{IH1,2}$	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)1,2}$	Input hysteresis voltage		0.25			V
$V_{ICL1,2}$	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		V
V_{DEL}	DE low level voltage				0.9	V
I_{DEL}	DE low level current	V_{IN} = 0.9 V	1			µA
V_{DEH}	DE high level voltage		2.1			V
I_{DEH}	DE high level current	V_{IN} = 2.1 V			10	µA
$V_{DE(hyst)}$	DE hysteresis voltage		0.25			V
V_{DECL}	DE clamp voltage	I_{DE} = 1 mA	5.5		7	V
		I_{DE} = -1 mA		-0.7		V

Table 8. Protections and diagnostics [1]

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	Short circuit current	V_{CC} = 13 V 5 V < V_{CC} < 24 V	65	90	130 130	A A
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 13 V; $T_R < T_j < T_{TSD}$		40		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS}+1	T_{RS}+5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; V_{IN} = 0; L = 6 mH	V_{CC}-28	V_{CC}-32	V_{CC}-35	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 1 A; T_j = -40 °C to 150 °C (see *Figure 8*)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 5 A; V_{SENSE} = 4 V; V_{DE} = 5 V; T_j = -40 °C...150 °C T_j = 25 °C...150 °C	11420 12130	17580 17580	23740 23030	—
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A; V_{SENSE} = 4 V; V_{DE} = 5 V; T_j = -40 °C...150 °C T_j = 25 °C...150 °C	11830 12680	16910 16910	21990 21140	—
dK_1/K_1 [1]	Current sense ratio drift	I_{OUT} =10 A; V_{SENSE} = 4 V; V_{DE} = 5 V; T_j = -40 °C to 150 °C	-14		+14	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 15 A; V_{SENSE} = 4 V; V_{DE}= 5 V; T_j = -40 °C...150 °C T_j = 25 °C...150 °C	11760 13040	16110 16110	20460 19180	—
dK_2/K_2 [1]	Current sense ratio drift	I_{OUT} = 15 A; V_{SENSE} = 4 V; V_{DE} = 5 V; T_j = -40 °C to 150 °C	-10		+10	%

Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 30 A; V_{SENSE} = 4 V; V_{DE} = 5 V; T_j = -40 °C...150 °C T_j = 25 °C...150 °C	13040 13810	15520 15520	18000 17230	—
dK_3/K_3(1)	Current sense ratio drift	I_{OUT} = 30 A; V_{SENSE} = 4 V; V_{DE} = 5 V; T_j = -40 °C to 150 °C	-5		+5	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{DE} = 0 V; V_{IN} = 0 V; T_j = -40 °C...150 °C	0		1	µA
		I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{DE} = 5 V; V_{IN} = 5 V; T_j = -40 °C...150 °C	0		2	µA
		I_{OUT} = 15 A; V_{SENSE} = 0 V; V_{DE} = 0 V; V_{IN} = 5 V;	0		1	µA
I_{OL}	Open-load on-state current detection threshold	V_{IN} = 5 V; 8 V < V_{CC} < 18 V I_{SENSE} = 5 µA	10		150	mA
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 45 A; V_{CSD} = 0 V; R_{SENSE} = 3.9 kΩ	5			V
V_{SENSEH}	Analog sense output voltage in fault condition(2)	V_{CC} =13 V; R_{SENSE} = 3.9 kΩ		8		V
I_{SENSEH}	Analog sense output current in fault condition(2)	V_{CC} =13 V; V_{SENSE} = 5 V		9		mA
$t_{DSENSE1H}$	Delay response time from rising edge of DE pin	V_{SENSE} < 4 V, 5 A < I_{out} < 30 A I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 4*)		50	100	µs
$t_{DSENSE1L}$	Delay response time from falling edge of DE pin	V_{SENSE} < 4 V, 5 A < I_{out} < 30 A I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 4*)		5	20	µs
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE} < 4 V, 5 A < I_{out} < 30 A I_{SENSE} = 90 % of $I_{SENSE\ max}$ V_{DE} = 5 V (see *Figure 4*)		200	600	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE} < 4 V, 5 A < I_{out} < 30 A I_{SENSE} = 10 % of $I_{SENSE\ max}$ V_{DE} = 5 V (see *Figure 4*)		100	250	µs

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation, overtemperature and open-load off-state detection.

Table 10. Open-load detection ($8V<V_{CC}<18V$, $V_{DE}= 5V$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load off-state voltage detection threshold	V_{IN} = 0 V, V_{DE} = 5 V; See *Figure 5*	2	—	4	V
t_{DSTKON}	Output short circuit to V_{CC} detection delay at turn off	V_{DE} = 5 V; See *Figure 5*	180	—	1200	µs
$I_{L(off2)r}$	Off-state output current at V_{OUT} = 4 V	V_{IN} = 0 V; V_{SENSE} = 0 V; V_{DE} = 5 V; V_{OUT} rising from 0 V to 4 V	-120	—	90	µA
$I_{L(off2)f}$	Off-state output current at V_{OUT} = 2 V	V_{IN} = 0 V; V_{SENSE} = V_{SENSEH} V_{DE} = 5 V; V_{OUT} falling from V_{CC} to 2 V	-50	—	90	µA
td_vol	Delay response from output rising edge to V_{SENSE} rising edge in open-load	V_{OUT} = 4 V; V_{IN} = 0 V; V_{DE} = 5 V; V_{SENSE} = 90 % of V_{SENSEH}		—	20	µs
td_voh	Delay response from output falling edge to V_{SENSE} falling edge in open-load	V_{OUT} = 2 V; V_{IN} = 0V; V_{DE} = 5 V; V_{SENSE} = 10 % of V_{SENSEH}		—	20	µs

Figure 4. Current sense delay characteristics

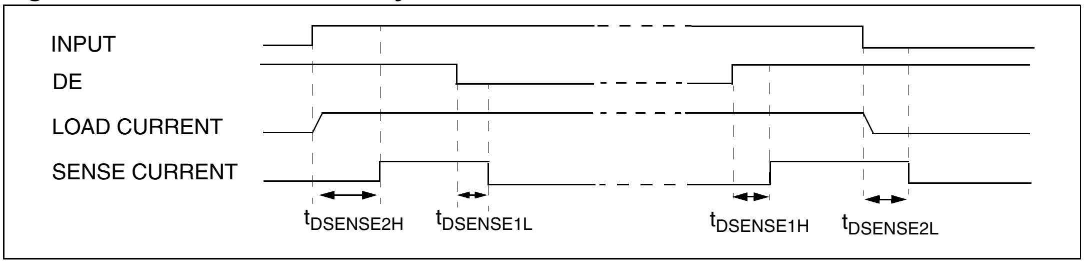


Figure 5. Open-load off-state delay timing

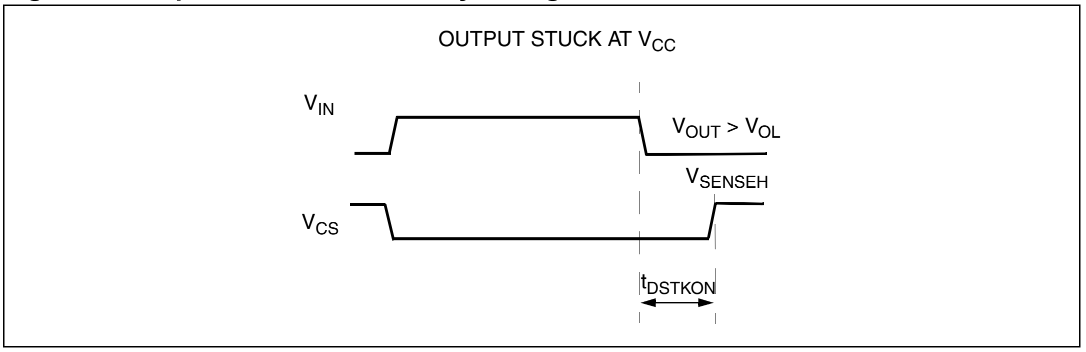


Figure 6. Switching characteristics

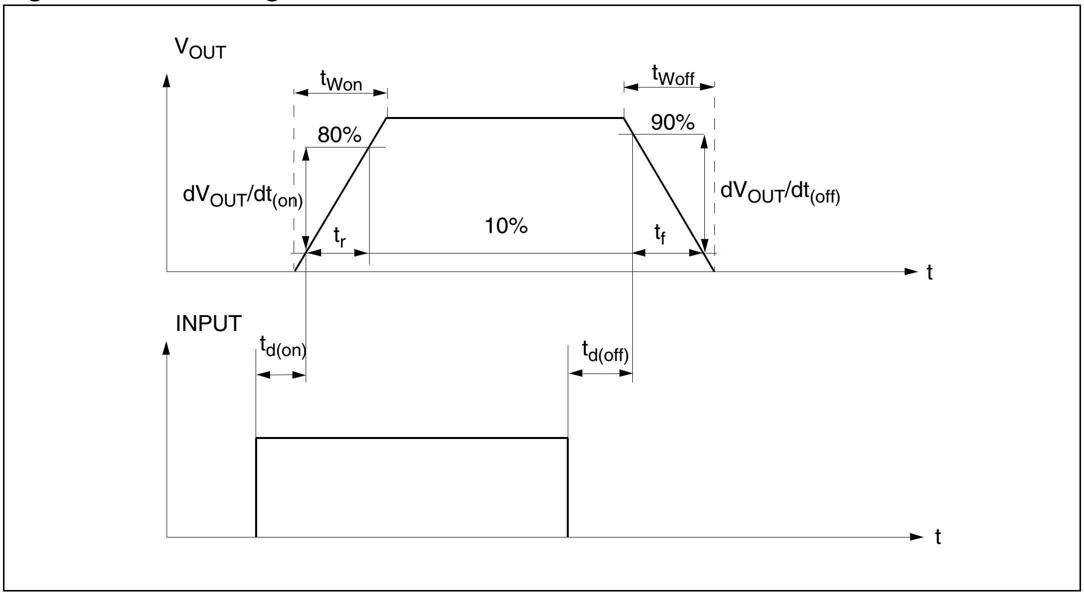


Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

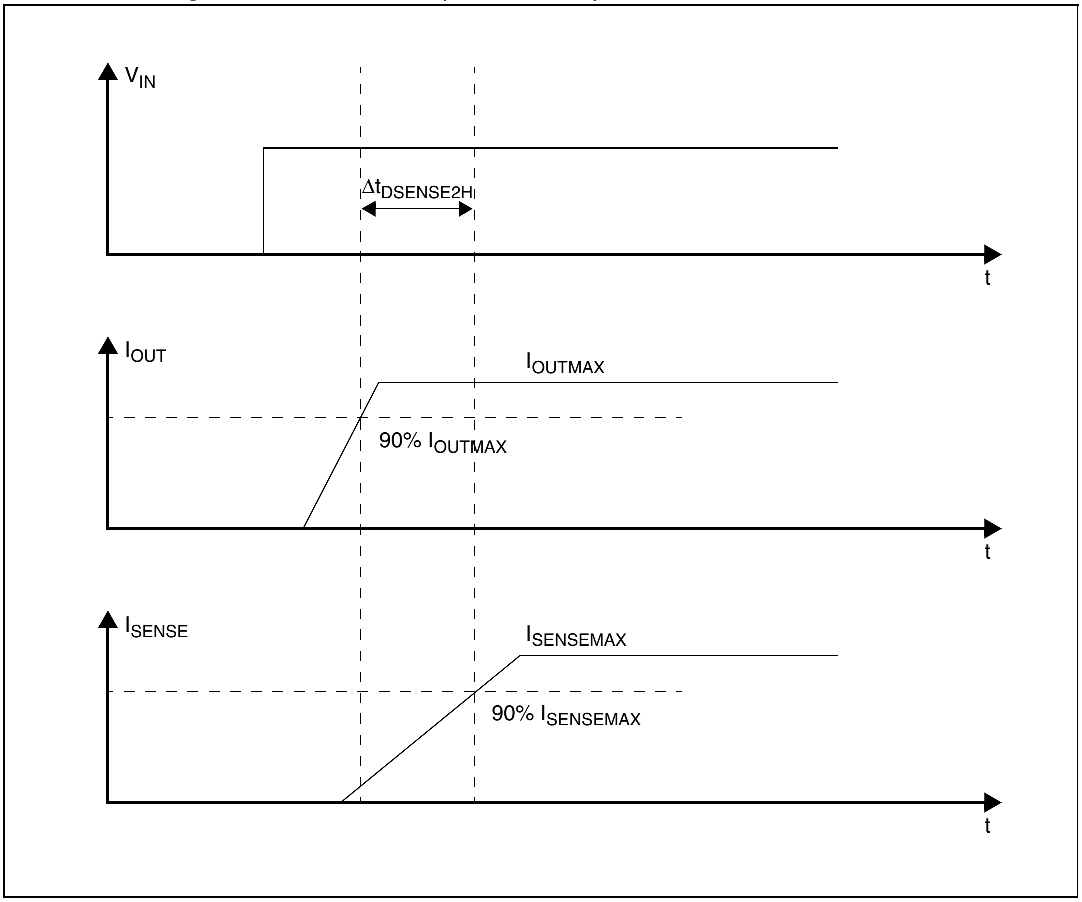


Figure 8. Output voltage drop limitation

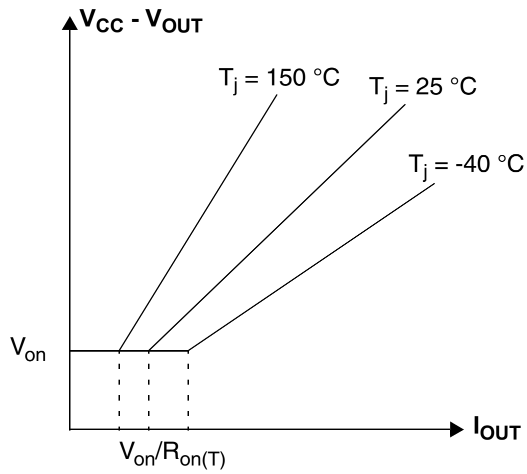
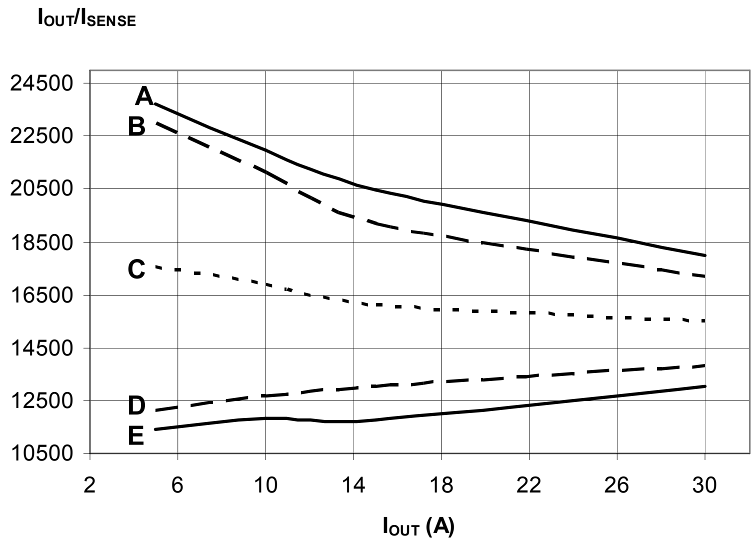


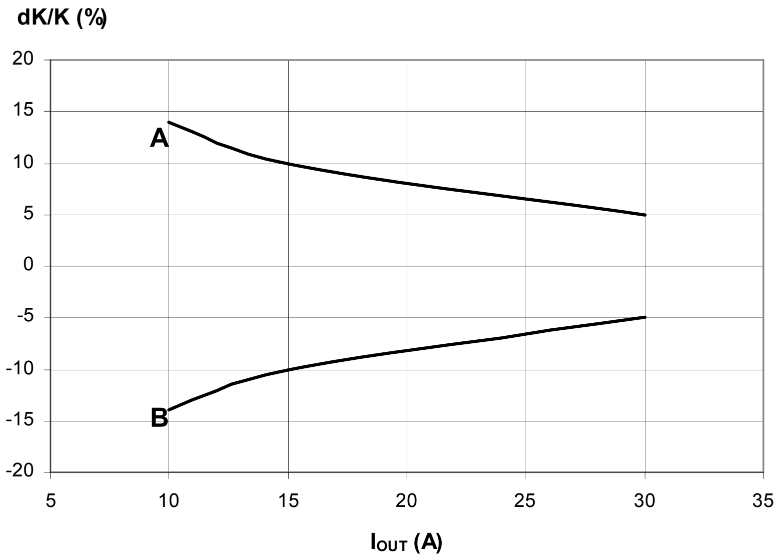
Figure 9. I_{OUT}/I_{SENSE} vs I_{OUT}



Legend:

A: Max, T_j = -40 °C to 150 °C
B: Max, T_j = 25 °C to 150 °C
C: Typical, T_j = -40 °C to 150 °C
D: Min, T_j = 25 °C to 150 °C
E: Min, T_j = -40 °C to 150 °C

Figure 10. Maximum current sense ratio drift vs load current(1)



Legend:

A: Max, T_j = -40 °C to 150 °C
B: Max, T_j = 25 °C to 150 °C

1. Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Enable	Input	Output	Sense (V_{DE}=5V)(1)
Normal operation	H H	L H	L H	0 Nominal
Overtemperature	H H	L H	L L	0 V_{SENSEH}
Undervoltage	H H	L H	L L	0 0
Overload	H H	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short circuit to GND (Power limitation)	H H	L H	L L	0 V_{SENSEH}
Open-load off-state (with external pull up)	H	L	H	V_{SENSEH}
Short circuit to V_{CC} (external pull up disconnected)	H H	L H	H H	V_{SENSEH} < Nominal
Negative output voltage clamp	H	L	L	0

1. If the V_{DE} is low, the SENSE output is at a high impedance; its potential depends on leakage currents and external circuit.

Table 12. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) Test pulse	Test levels[1]		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b[2]	+65 V	+87 V	1 pulse			400 ms, 2 Ω

Table 13. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004(E) Test pulse	Test level results[1]	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b[2] [3]	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b
2. Valid in case of external load dump clamp: 40V maximum referred to ground.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in *Table 3*.

Table 14. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 11. Normal operation

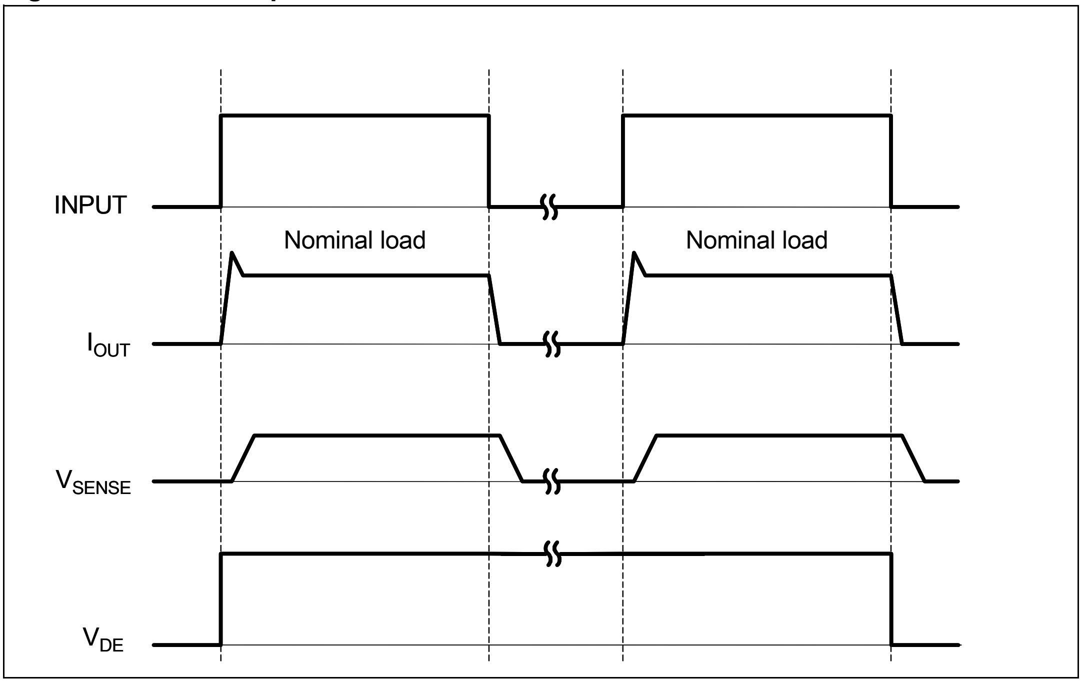


Figure 12. Overload or short to GND

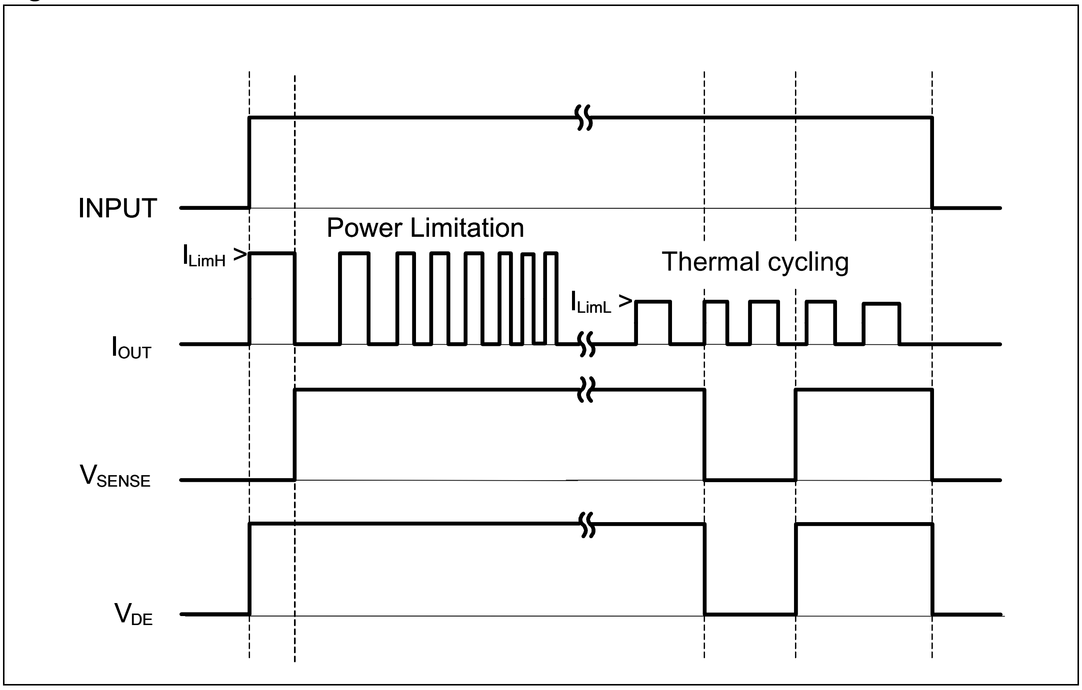


Figure 13. Intermittent overload

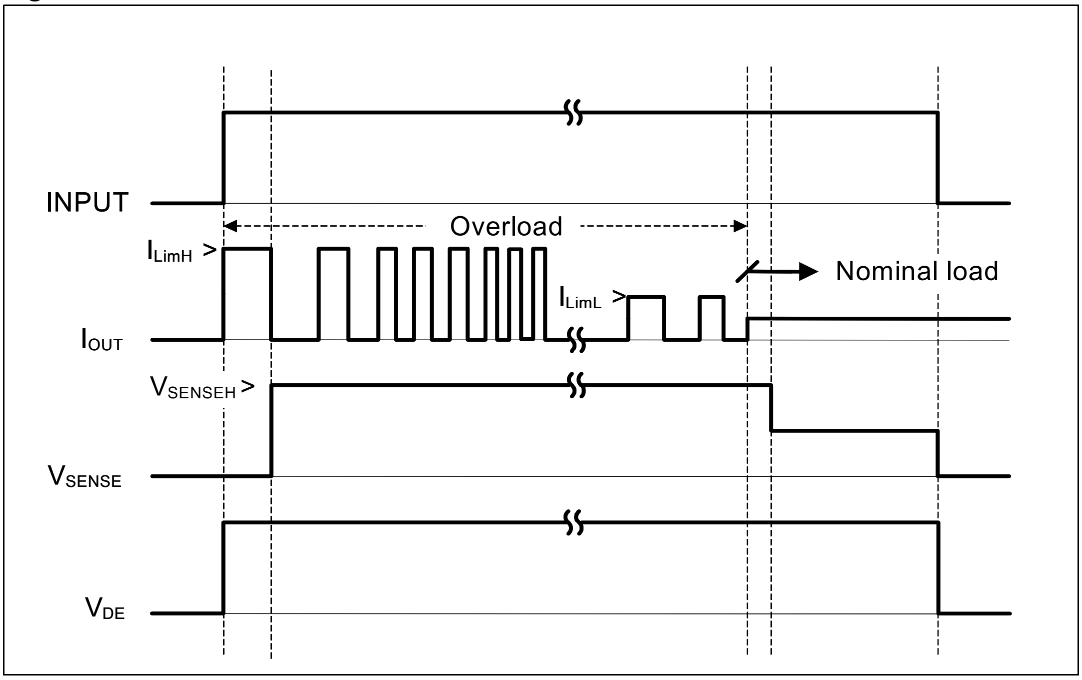


Figure 14. Off-state open-load with external circuitry

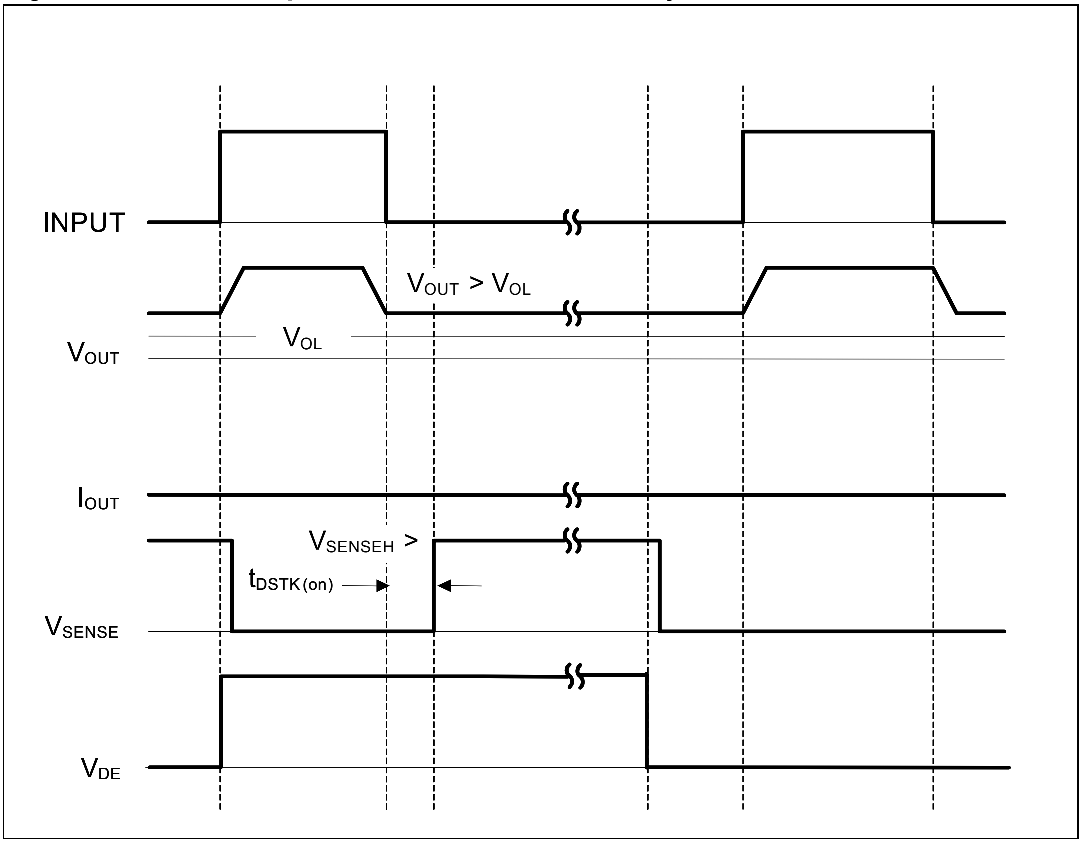


Figure 15. Short to V_{CC}

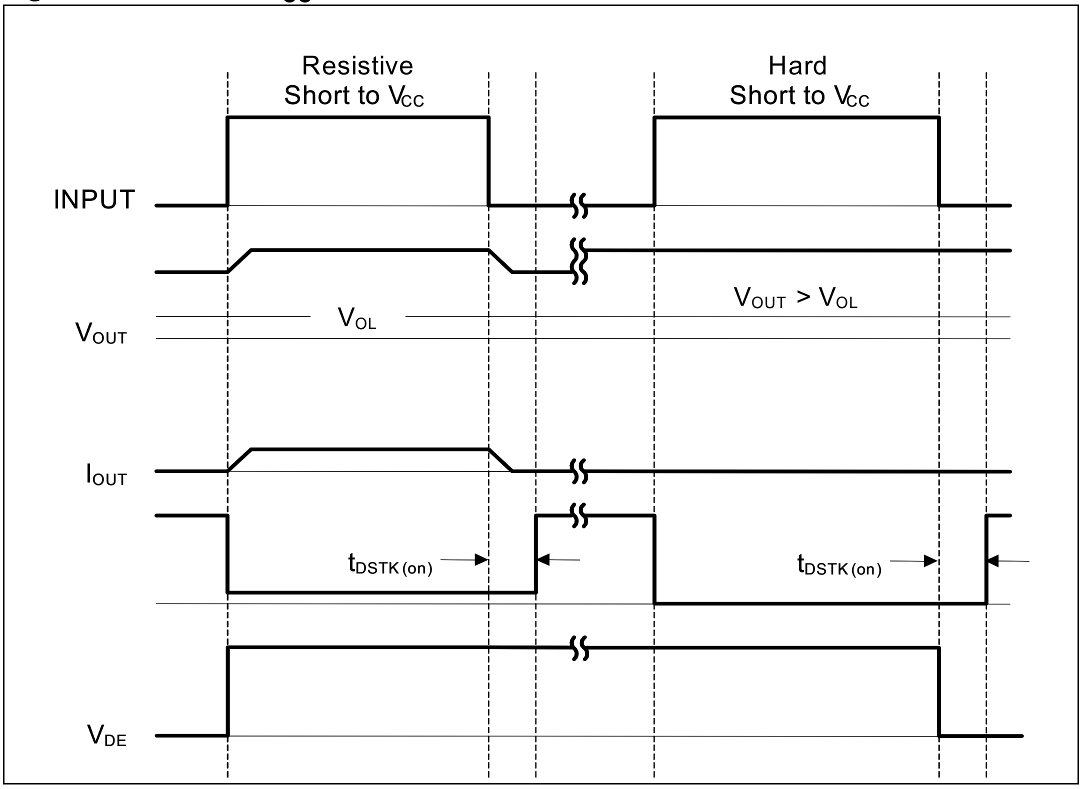
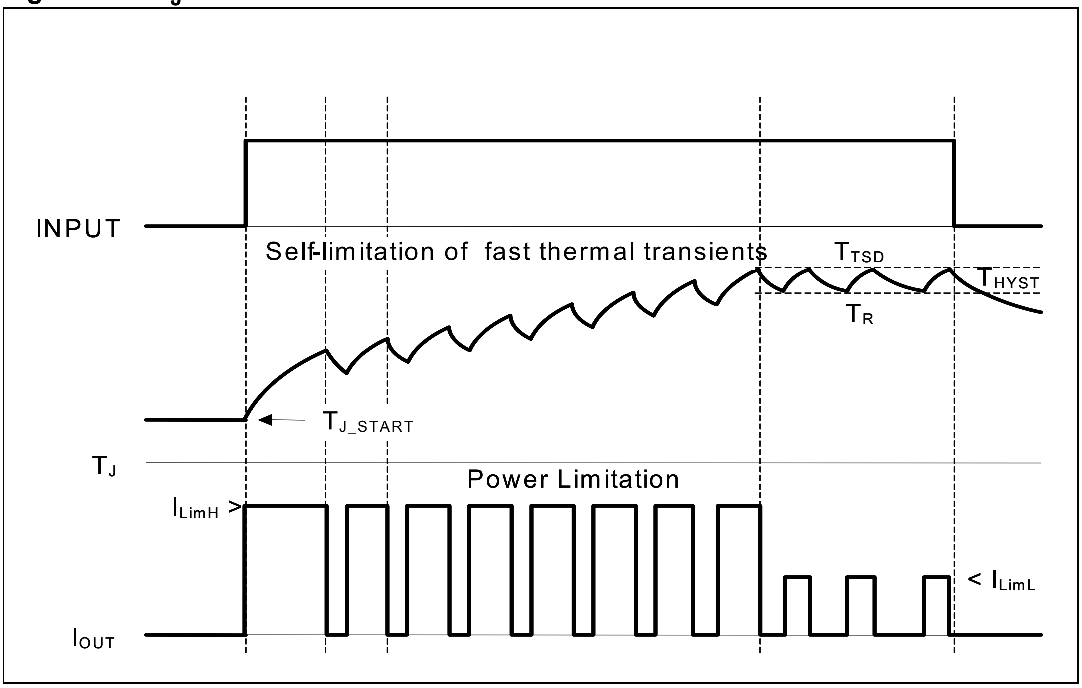


Figure 16. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 17. Off-state output current

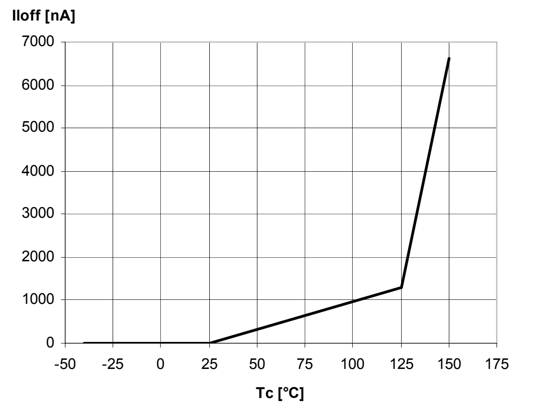


Figure 18. High level input current

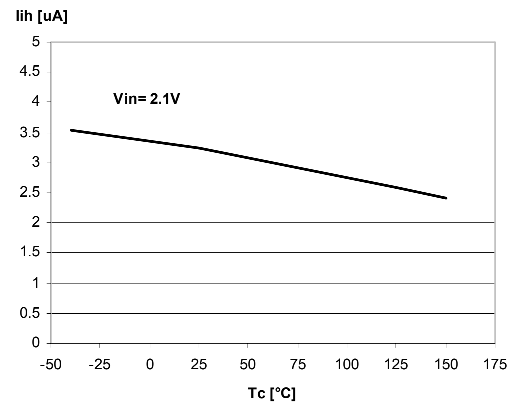


Figure 19. Input clamp voltage

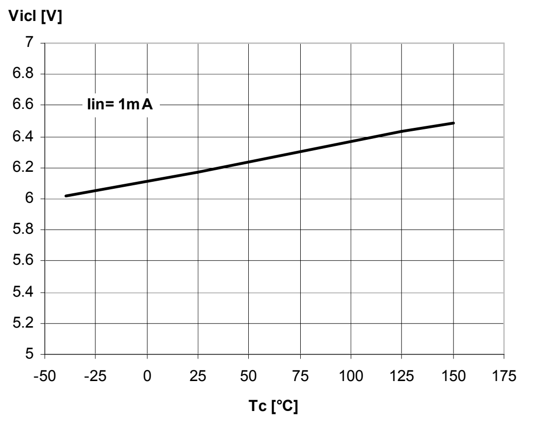


Figure 20. Input low level voltage

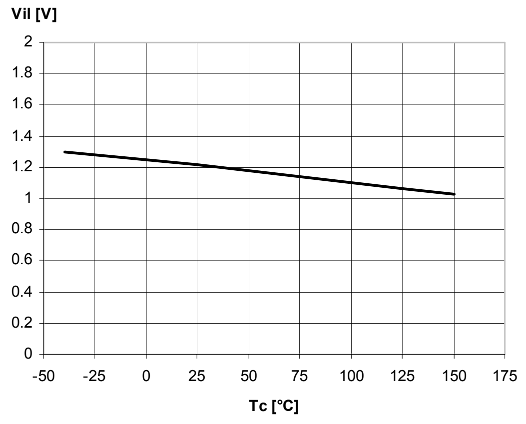


Figure 21. Input high level voltage

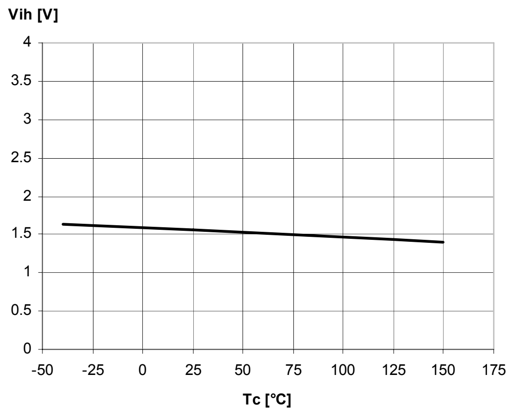


Figure 22. Input hysteresis voltage

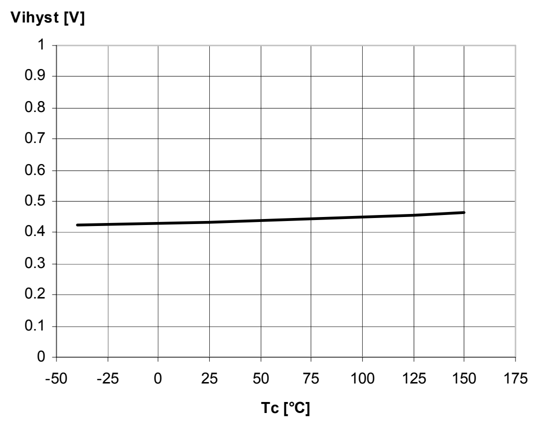


Figure 23. On-state resistance vs T_{case}

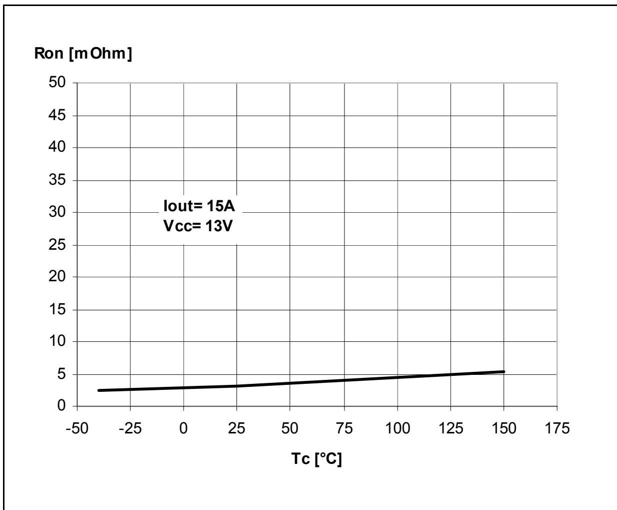


Figure 24. On-state resistance vs V_{CC}

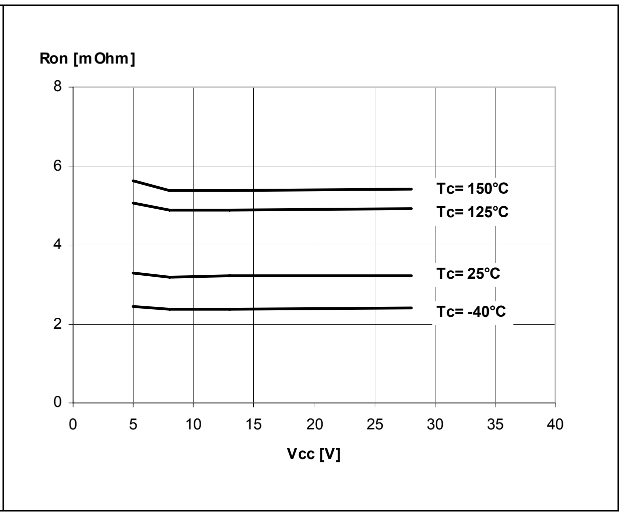


Figure 25. Undervoltage shutdown

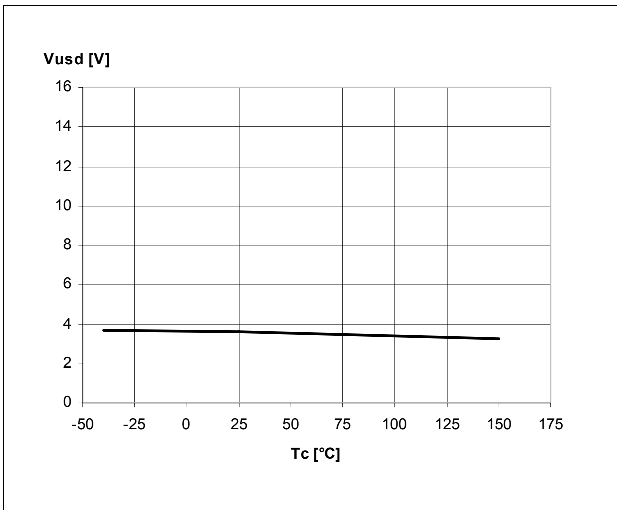


Figure 26. Turn-on voltage slope

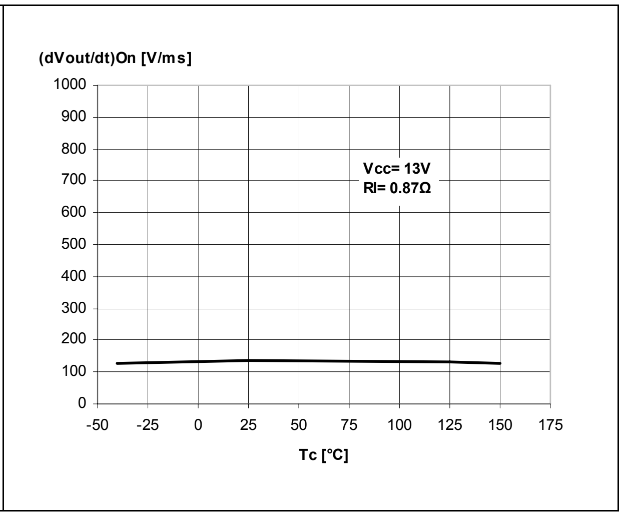


Figure 27. I_{LIMH} vs T_{case}

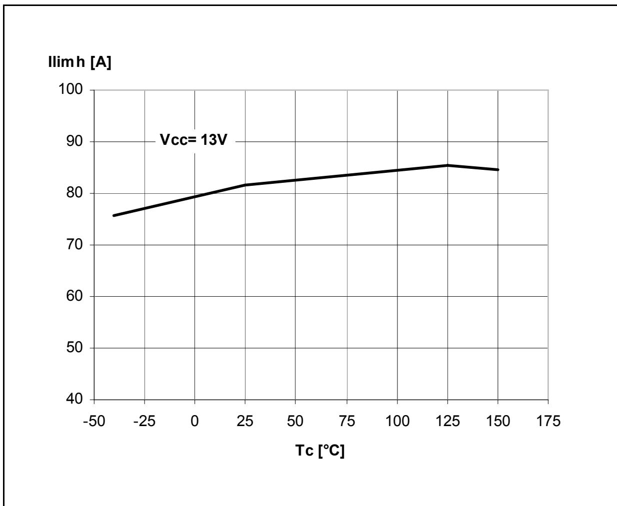


Figure 28. Turn-off voltage slope

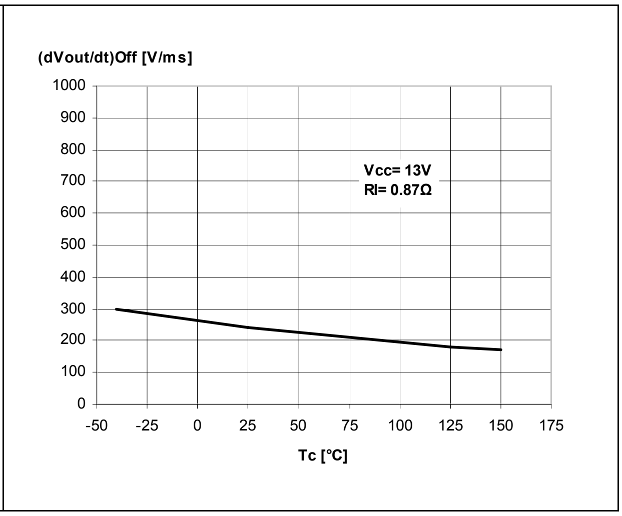


Figure 29. DE high level voltage

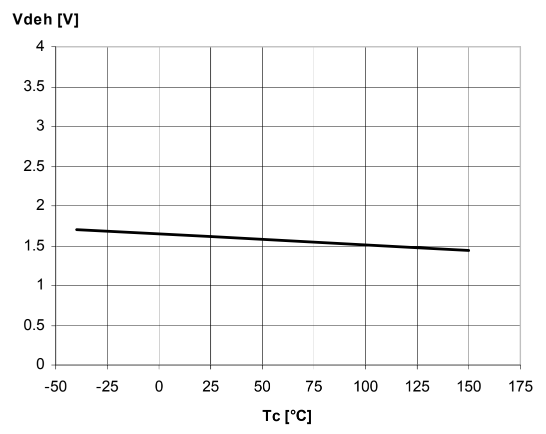


Figure 30. DE clamp voltage

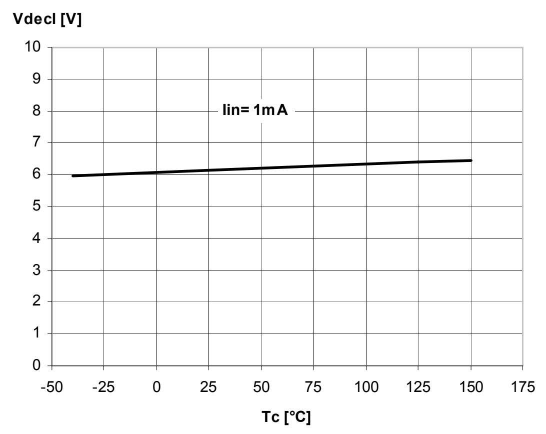
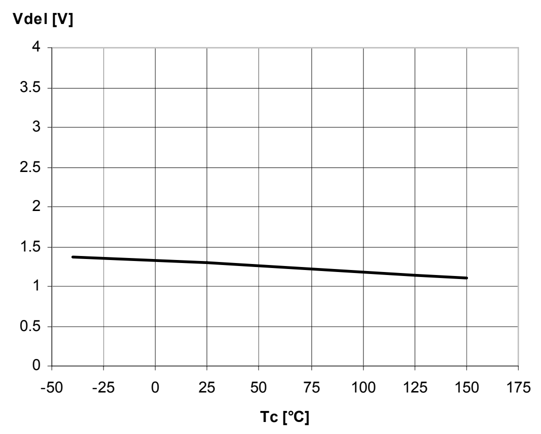
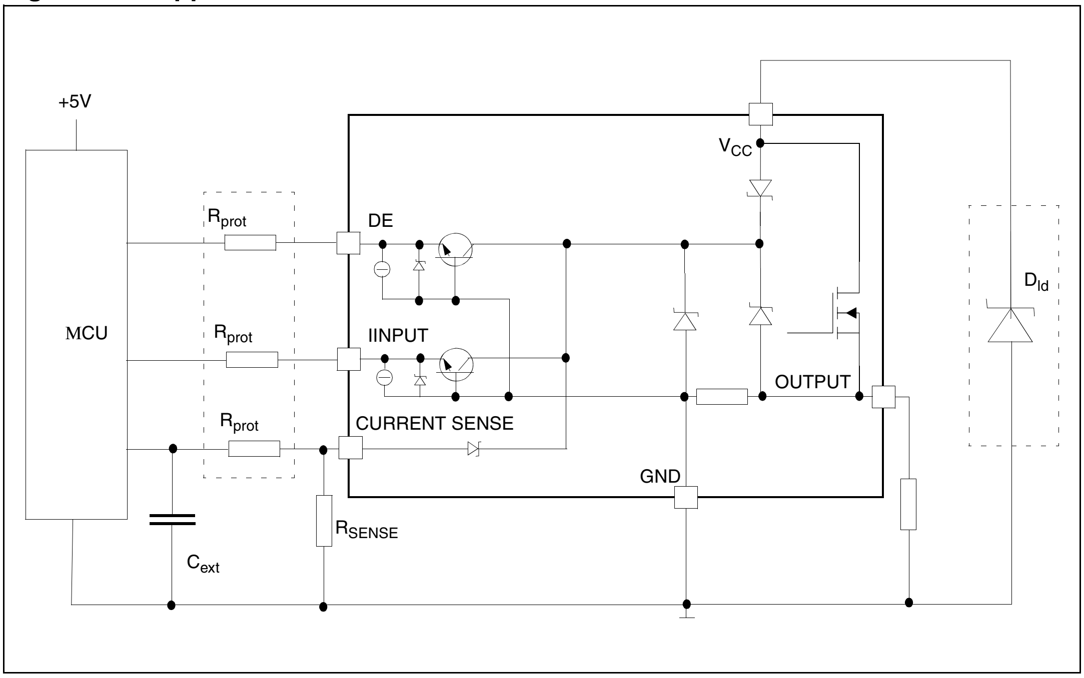


Figure 31. DE low level voltage



3 Application information

Figure 32. Application schematic



3.1 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pins are pulled negative to approximately -1.5V.

ST suggests the insertion of resistors (R_{prot}) in the lines to prevent the microcontroller I/O pins from latching up.

The values of these resistors provide a compromise between the leakage current of the microcontroller, the current required by the HSD I/Os (input levels compatibility) and the latch-up limit of the microcontroller I/Os.

$-V_{CCpeak}/I_{latchup} \le R_{prot} \le (V_{OH\mu C}-V_{IH}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 1.5V and $I_{latchup} \ge$ 20mA; $V_{OH\mu C} \ge$ 4.5V

$75\Omega \le R_{prot} \le 240k\Omega$.

Recommended values: R_{prot} =10kΩ, C_{EXT}=10nF

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CCPK} maximum rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

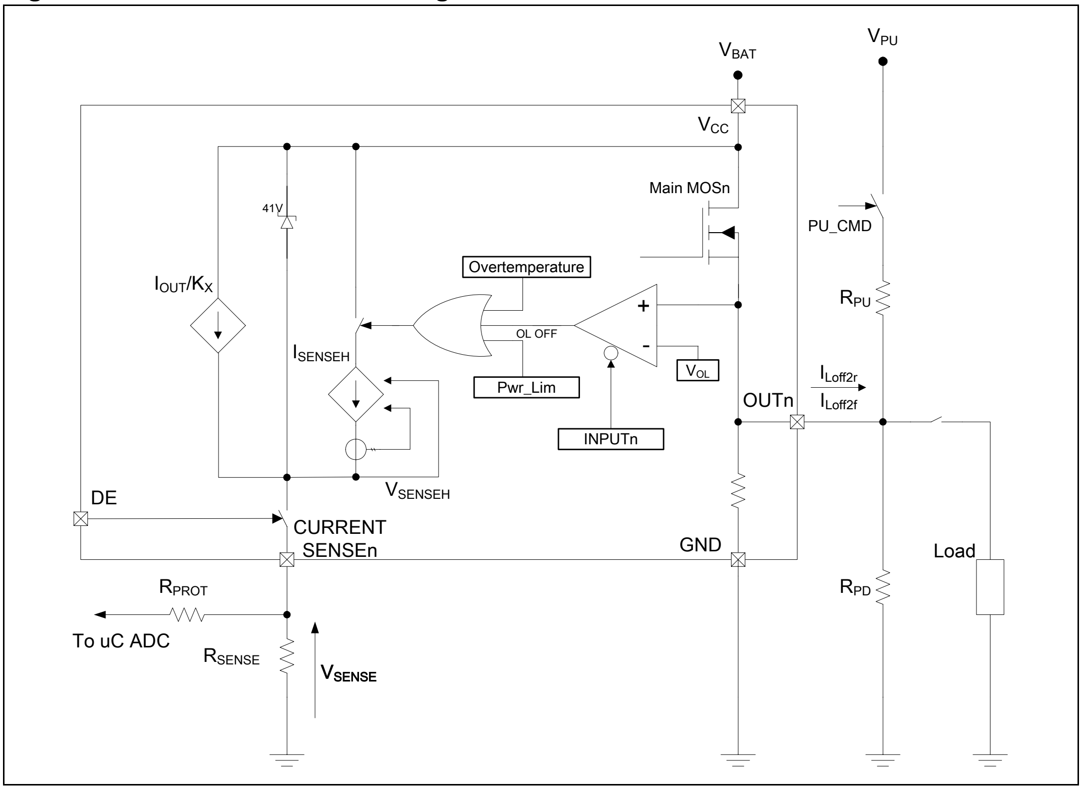
3.3 Current sense and diagnostic

The current sense pin performs a double function (see *Figure 33: Current sense and diagnostics*):

- **Current mirror of the load current in normal operation,** delivering a current proportional to the load current according to a known ratio $\mathbf{K_X}$.
  The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE}. Linearity between I_{OUT} and V_{SENSE} is ensured up to 5V minimum (see parameter V_{SENSE} in *Table 9: Current sense (8 V < V_{CC} < 18 V)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 9: Current sense (8 V < V_{CC} < 18 V)*).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Table 11: Truth table*):
  - Power limitation activation
  - Overtemperature
  - Short to V_{CC} in off-state
  - Open-load in off-state with additional external components.

A logic level low on the DE pin simultaneously sets all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing the sense resistance and ADC line among different devices.

Figure 33. Current sense and diagnostics



3.3.1 Short to V_{CC} and off-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Little or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

Off-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor (R_{PU}) connecting the output to a positive supply voltage (V_{PU}).

It is preferable that V_{PU} be switched off during the module standby mode to avoid an increase in the overall standby current consumption in normal conditions, that is, when the load is connected.

An external pull down resistor (R_{PD}) connected between output and GND is mandatory to avoid misdetection in case of floating outputs in off-state (see *Figure 33: Current sense and diagnostics*).

R_{PD} must be selected in order to ensure $V_{OUT} < V_{OLmin}$ unless pulled up by the external circuitry:

$$V_{OUT}\Big|_{Pull-up_OFF} = R_{PD} \cdot I_{L(off2)f} < V_{OL\min} = 2V$$

$R_{PD} \leq 22$ KΩ is recommended.

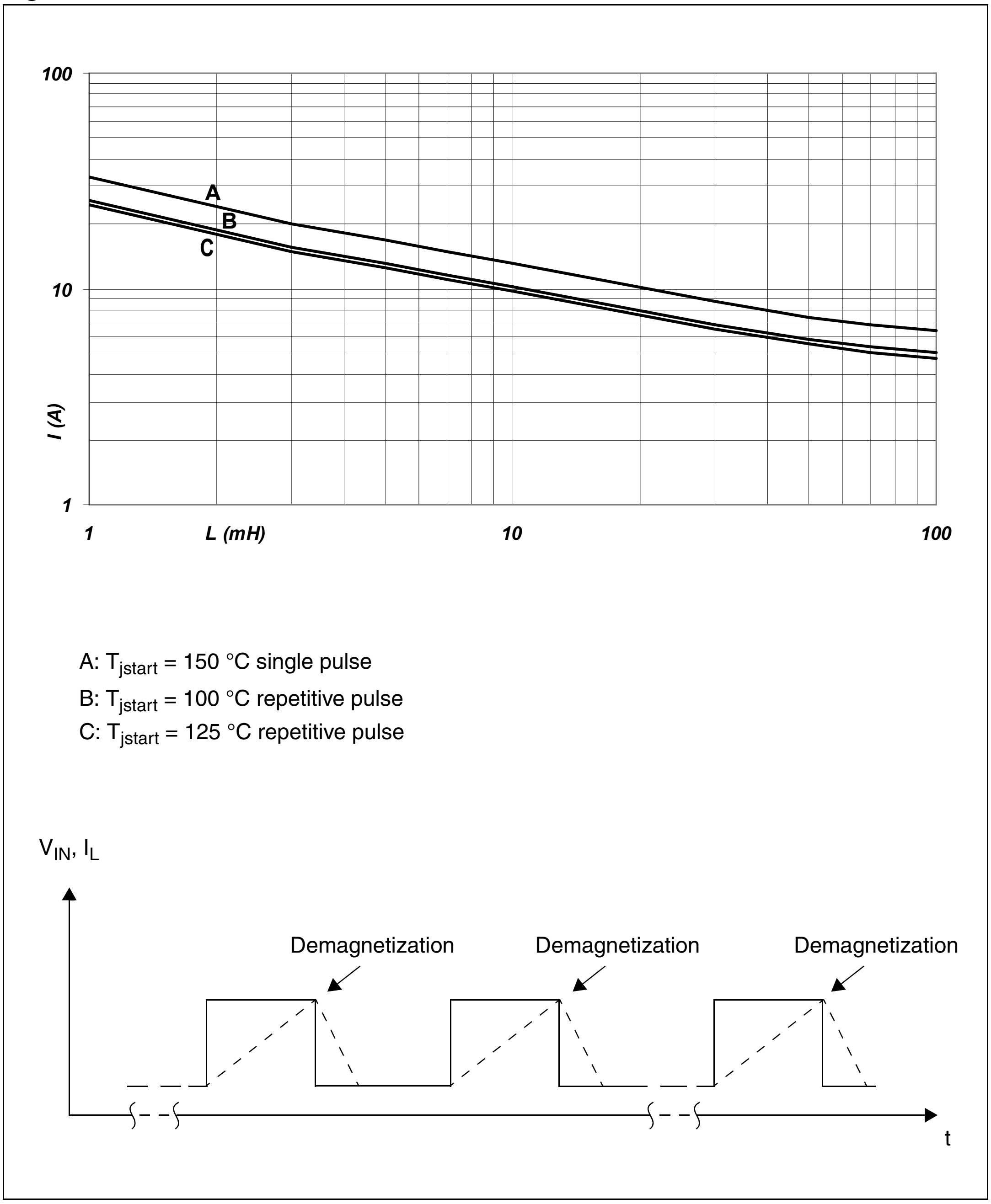
For proper open-load detection in off-state, the external pull-up resistor must be selected according to the following formula:

$$V_{OUT}\Big|_{Pull-up_ON} = \frac{R_{PD} \cdot V_{PU} - R_{PU} \cdot R_{PD} \cdot I_{L(off2)r}}{R_{PU} + R_{PD}} > V_{OL\max} = 4V$$

For the values of V_{OLmin},V_{OLmax}, $I_{L(off2)r}$ and $I_{L(off2)f}$ see *Table 10: Open-load detection (8V<V_{CC}<18V, VDE= 5V)*.

3.4 Maximum demagnetization energy (V_{CC} = 13.5V)

Figure 34. Maximum turn-off current versus inductance (1)

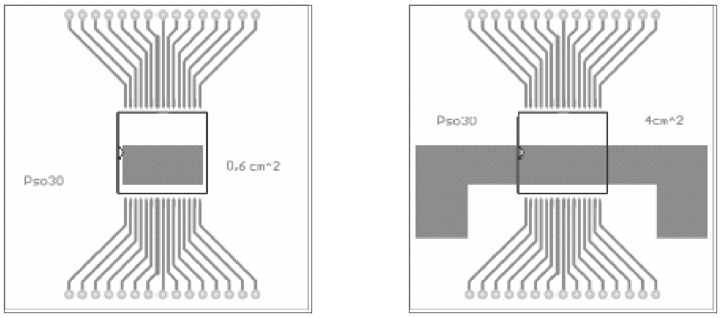


1. Values are generated with R_L = 0 Ω.
In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 MultiPowerSO-30 thermal data

Figure 35. MultiPowerSO-30 PC board(1)



1. Layout condition of R_{th} and Z_{th} measurements (PCB: double layer, thermal vias, FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 70 µm (front and back side), copper areas: from minimum pad lay-out to 16 cm^2).

Figure 36. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel ON)

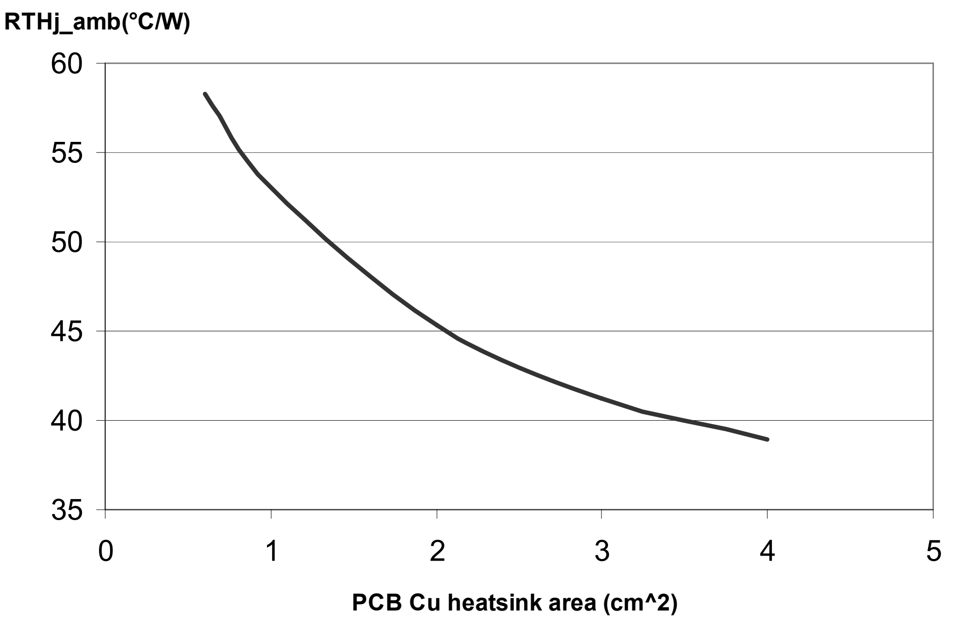


Figure 37. MultiPowerSO-30 thermal impedance junction ambient single pulse (one channel ON)

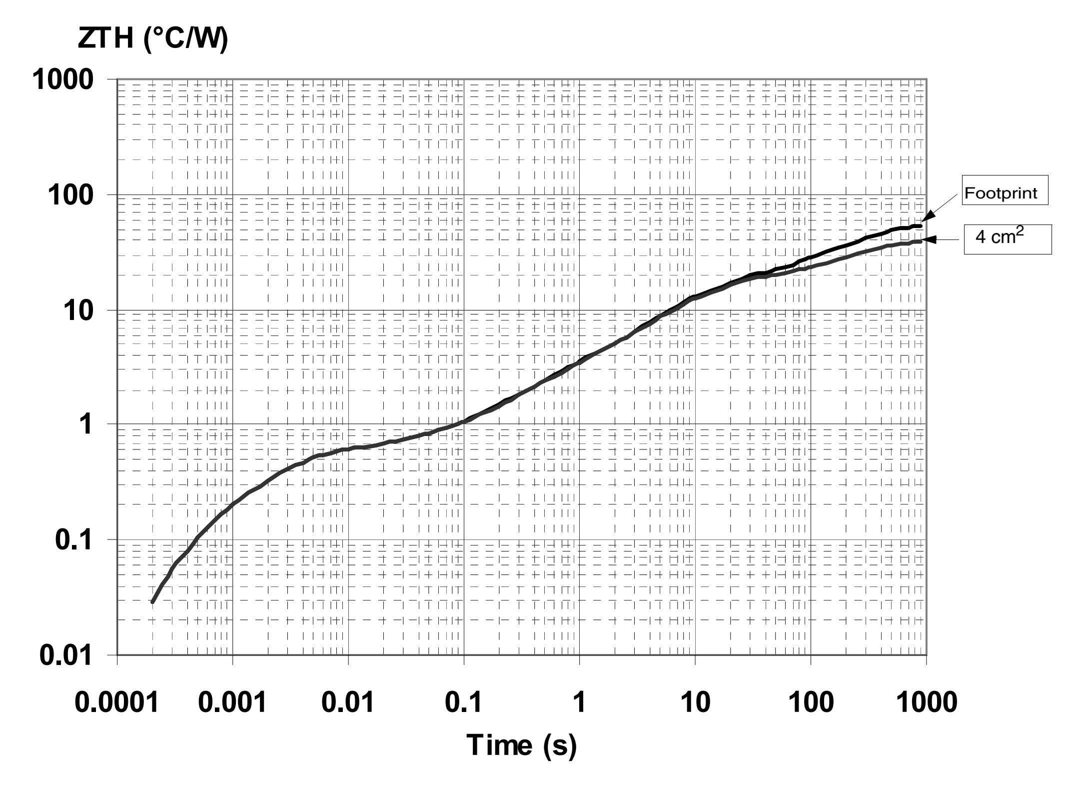
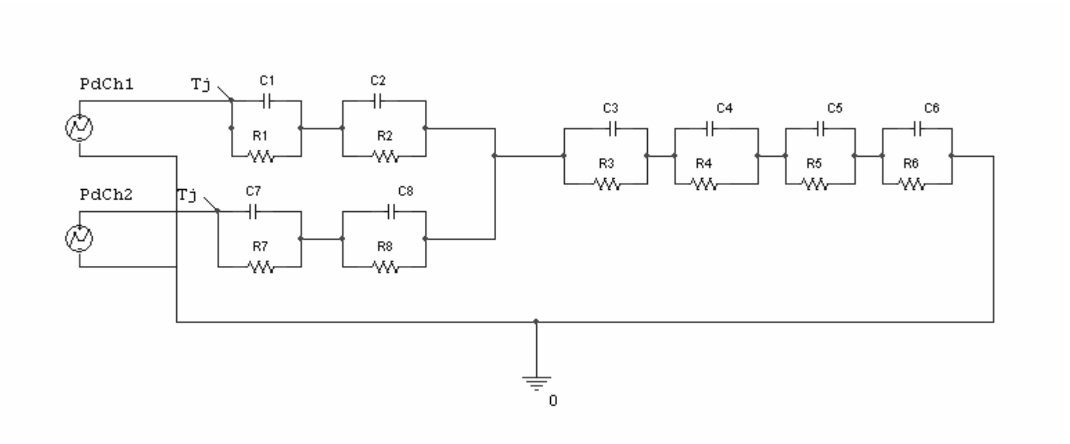


Figure 38. Thermal fitting model of a double channel HSD in MultiPowerSO-30(1)



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protection functions (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 1: Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

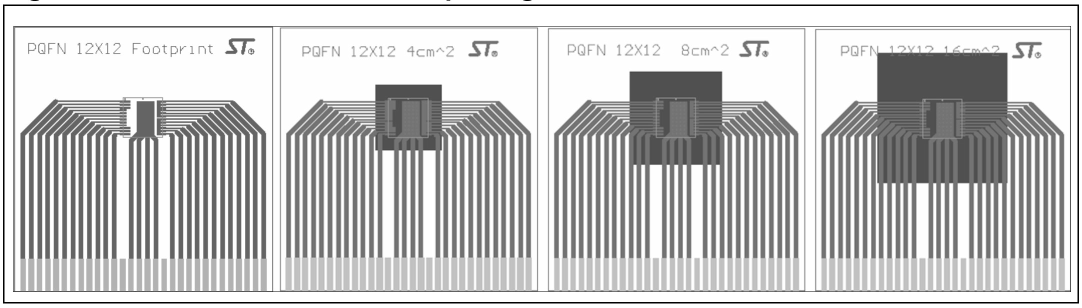
where $\delta = t_p / T$

Table 15. Thermal parameters for MultiPowerSO-30

Area/island (cm^2)	Footprint	4
R1 (°C/W)	0.05	
R2 (°C/W)	0.3	
R3 (°C/W)	0.5	
R4 (°C/W)	1.3	
R5 (°C/W)	14	
R6 (°C/W)	44.7	23.7
R7 (°C/W)	0.05	
R8 (°C/W)	0.3	
C1 (W.s/°C)	0.005	
C2 (W.s/°C)	0.008	
C3 (W.s/°C)	0.01	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.6	
C6 (W.s/°C)	5	11
C7 (W.s/°C)	0.005	
C8 (W.s/°C)	0.008	

4.2 PQFN - 12x12 power lead-less thermal data

Figure 39. 12x12 Power lead-less package PC board(1)



1. Layout condition of R_{th} and Z_{th} measurements (PCB: double layer, thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70 µm (front and back side), copper areas: minimum pad lay-out).

Figure 40. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel ON)

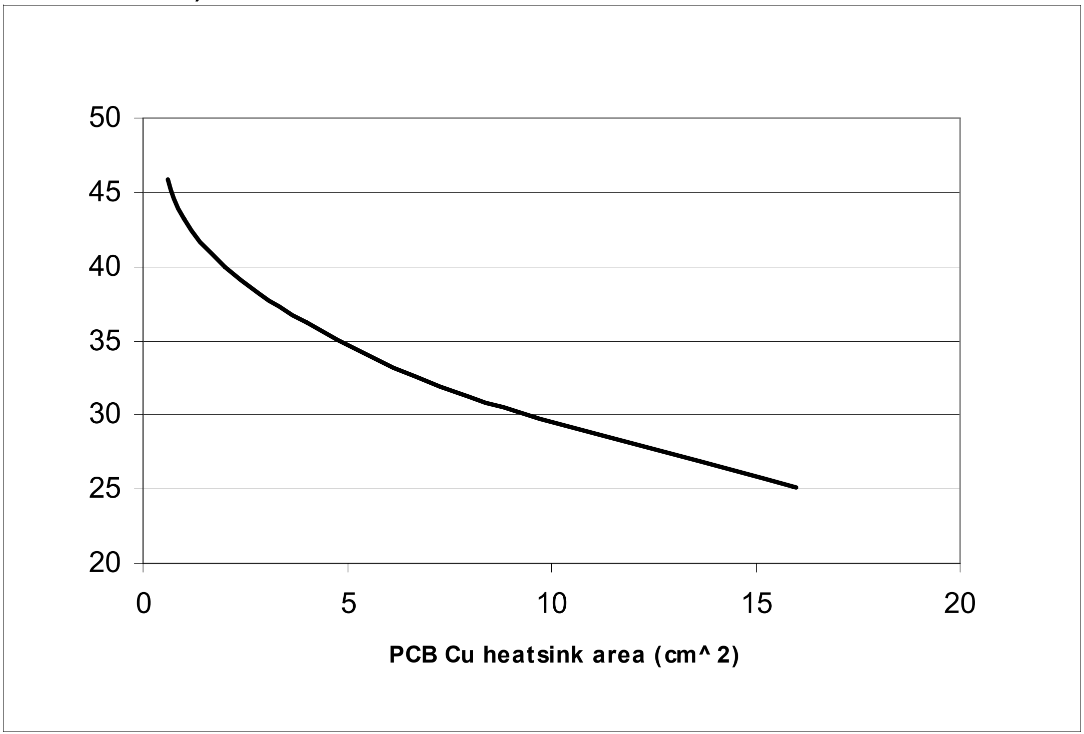


Figure 41. PQFN - 12x12 power lead-less package thermal impedance junction ambient single pulse (one channel ON)

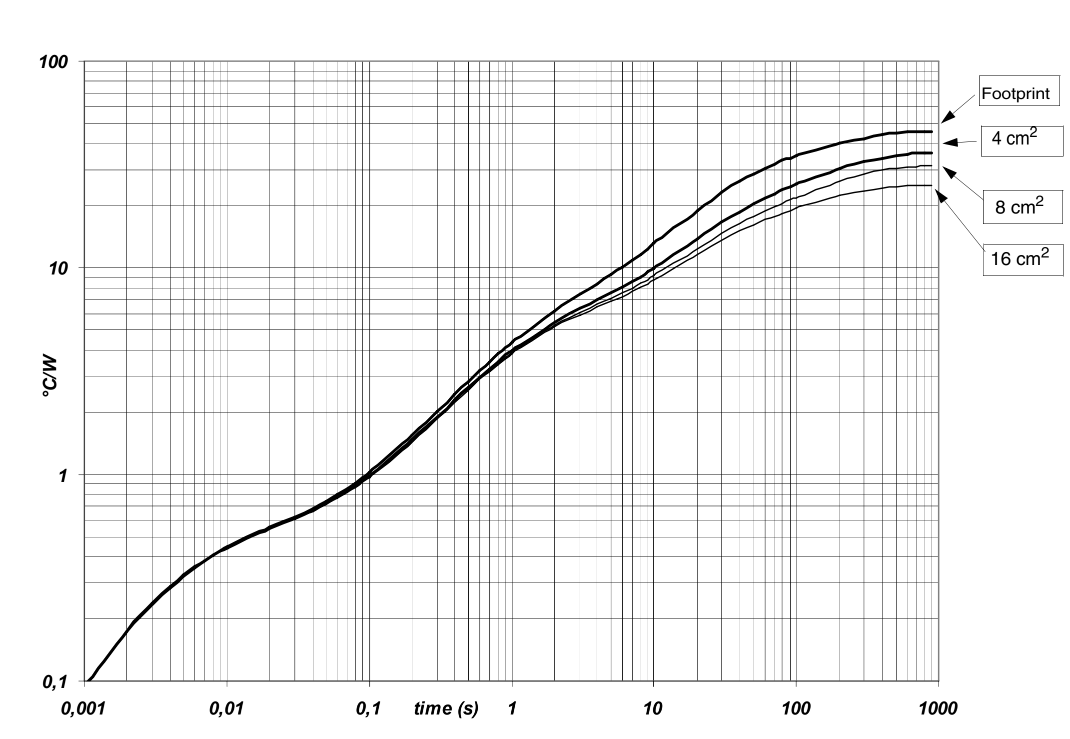
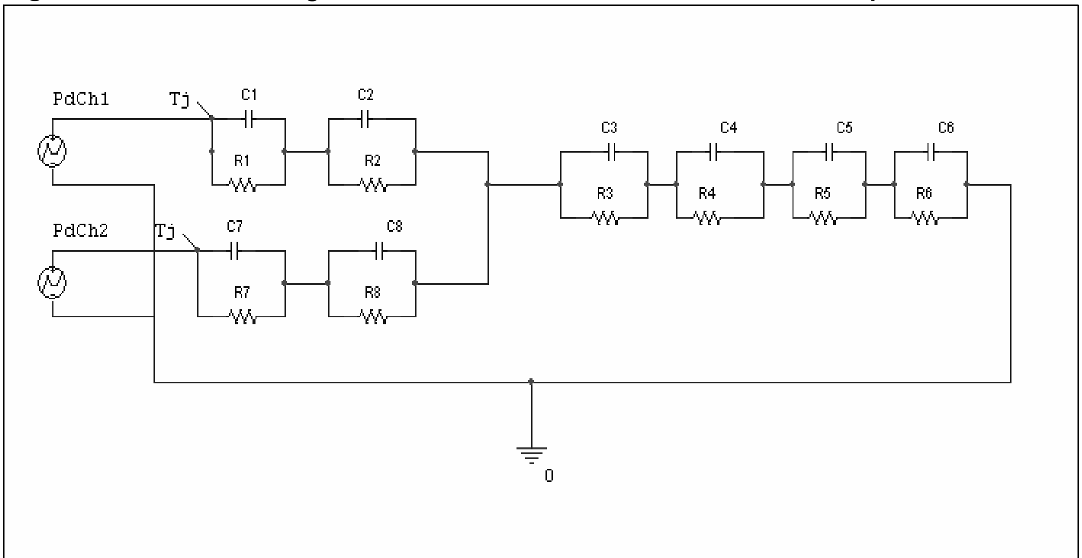


Figure 42. Thermal fitting model of a double channel HSD in PQFN - 12x12 power lead-less(1)



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protection functions (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_p / T$

Table 16. Thermal parameters for PQFN - 12x12 power lead-less

Area/island (cm^2)	Footprint	4	8	16
R1 (°C/W)	0.35			
R2 (°C/W)	0.15			
R3 (°C/W)	4.2			
R4 (°C/W)	9.6	9.4	9.2	9
R5 (°C/W)	15.1	10.5	8.5	5.5
R6 (°C/W)	16.7	12	9	6
R7 (°C/W)	0.35			
R8 (°C/W)	0.15			
C1 (W.s/°C)	0.018			
C2 (W.s/°C)	0.015			
C3 (W.s/°C)	0.2			
C4 (W.s/°C)	1.9	2.2	2.32	2.45
C5 (W.s/°C)	2.45	7.3	13.7	20
C6 (W.s/°C)	11.85	22	25	30
C7 (W.s/°C)	0.018			
C8 (W.s/°C)	0.015			

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 MultiPowerSO-30 mechanical data

Figure 43. MultiPowerSO-30 outline

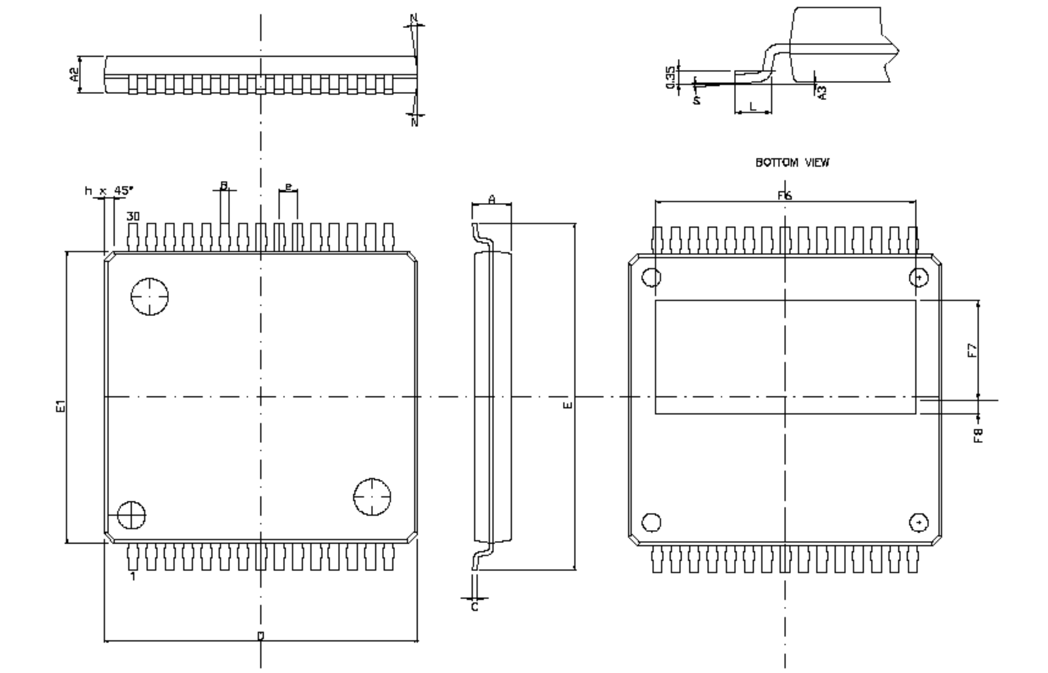


Table 17. MultiPowerSO-30 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.35
A2	1.85		2.25
A3	0		0.1
B	0.42		0.58
C	0.23		0.32
D	17.1	17.2	17.3
E	18.85		19.15
E1	15.9	16	16.1
“e”	1		
F6		14.3	
F7		5.45	
F8		0.73	
L	0.8		1.15
N			10 Deg
S	0 Deg		7 Deg

5.3 PQFN - 12x12 power lead-less mechanical data

Figure 44. PQFN - 12x12 power lead-less outline

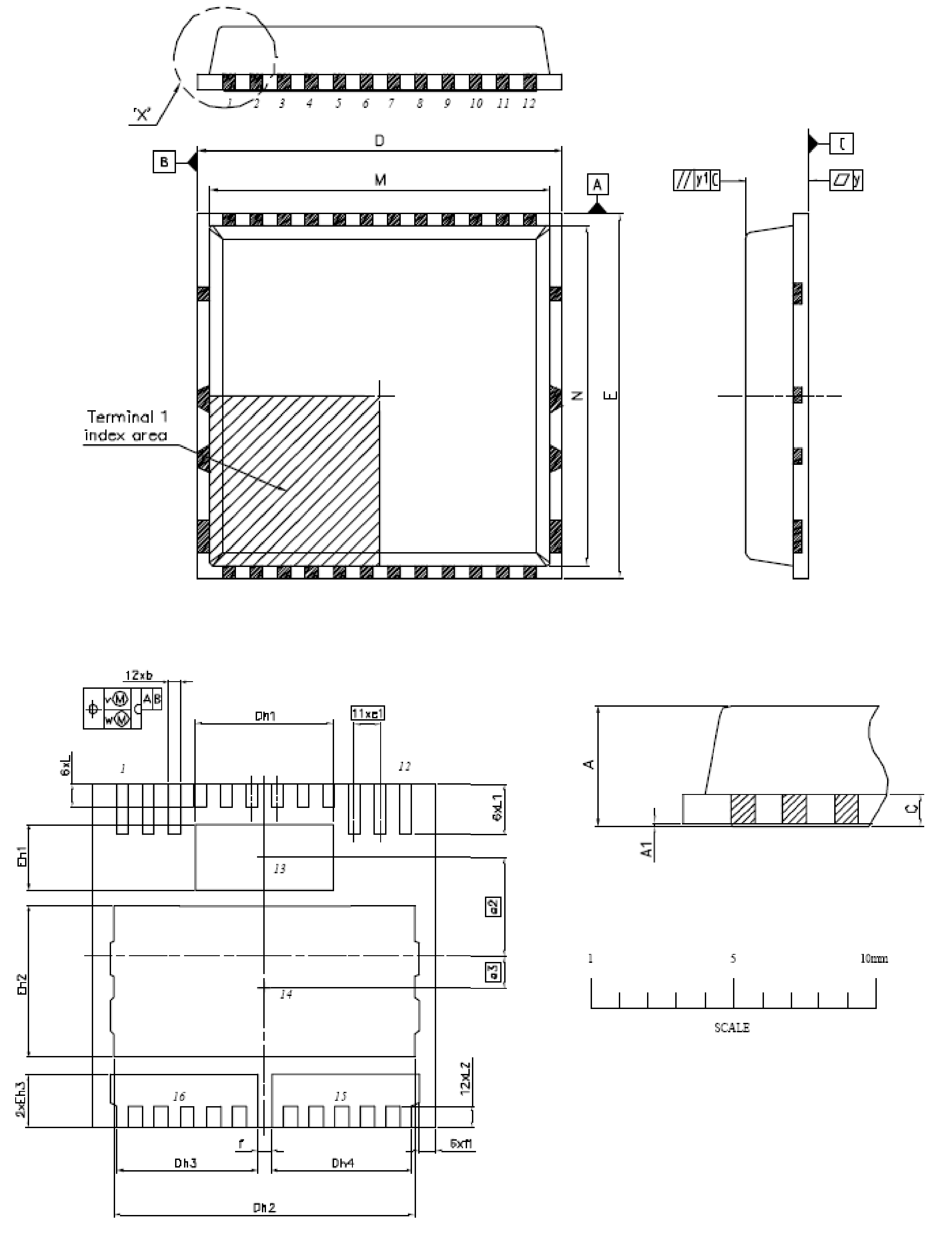


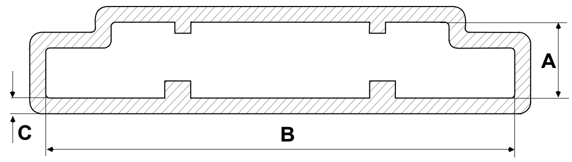
Table 18. PQFN - 12x12 power lead-less mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2		2.2
A1	0		0.05
b	0.35		0.47
C		0.50	
D	11.90		12.10
Dh1	4.65		4.95
Dh2	10.45		10.65
Dh3	4.80		5
Dh4	4.80		5
E	11.90		12.10
Eh1	2.15		2.45
Eh2	5.15		5.45
Eh3	1.70		2
e1		0.90	
e2		3.45	
e3		1.10	
f		0.50	
f1		0.60	
L	0.75		0.95
L1	1.65		1.90
L2	0.76		0.78
M	11.10		11.30
N	11.10		11.30
v		0.1	
w		0.05	
y		0.05	
y1		0.1	

5.4 MultiPowerSO-30 packing information

The devices can be packed in tube or tape and reel shipments (see *Table 19: Device summary*).

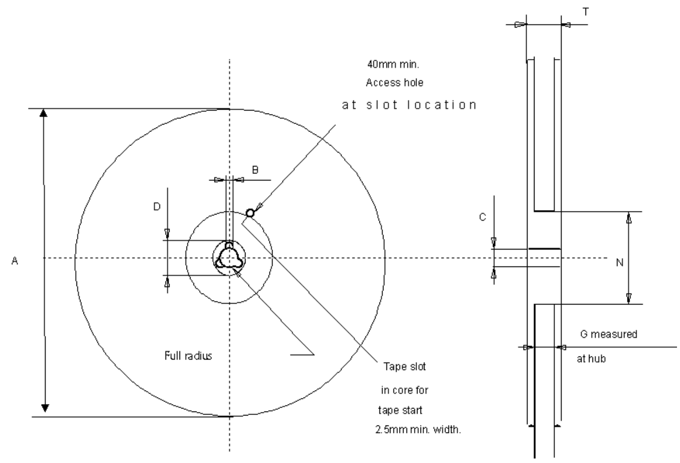
Figure 45. MultiPowerSO-30 tube shipment (no suffix)



Tube dimension

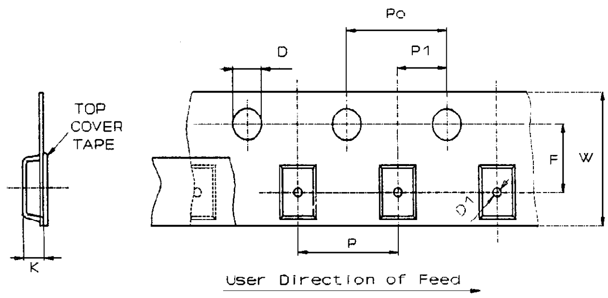
Dimension	mm
Base Q.ty	29
Bulk Q.ty	435
Tube length (± 0.5)	532
A	3.82
B	23.6
C (± 0.13)	0.8

Figure 46. MultiPowerSO-30 tape and reel shipment (suffix “TR”)



Reel dimension

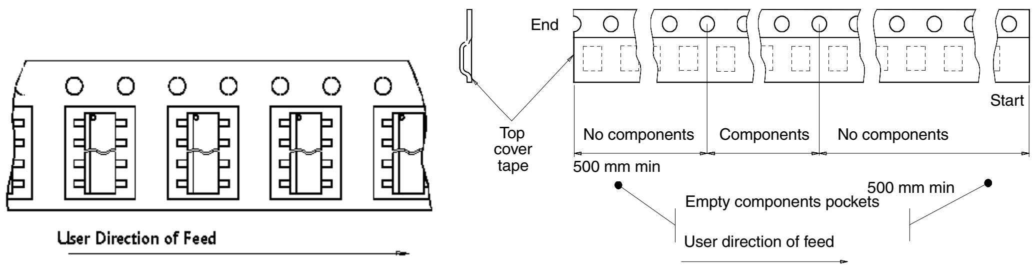
Dimension	mm
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
D (min)	20.2
G (+ 2 / -0)	32
N (min)	100
T (max)	38.4



Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

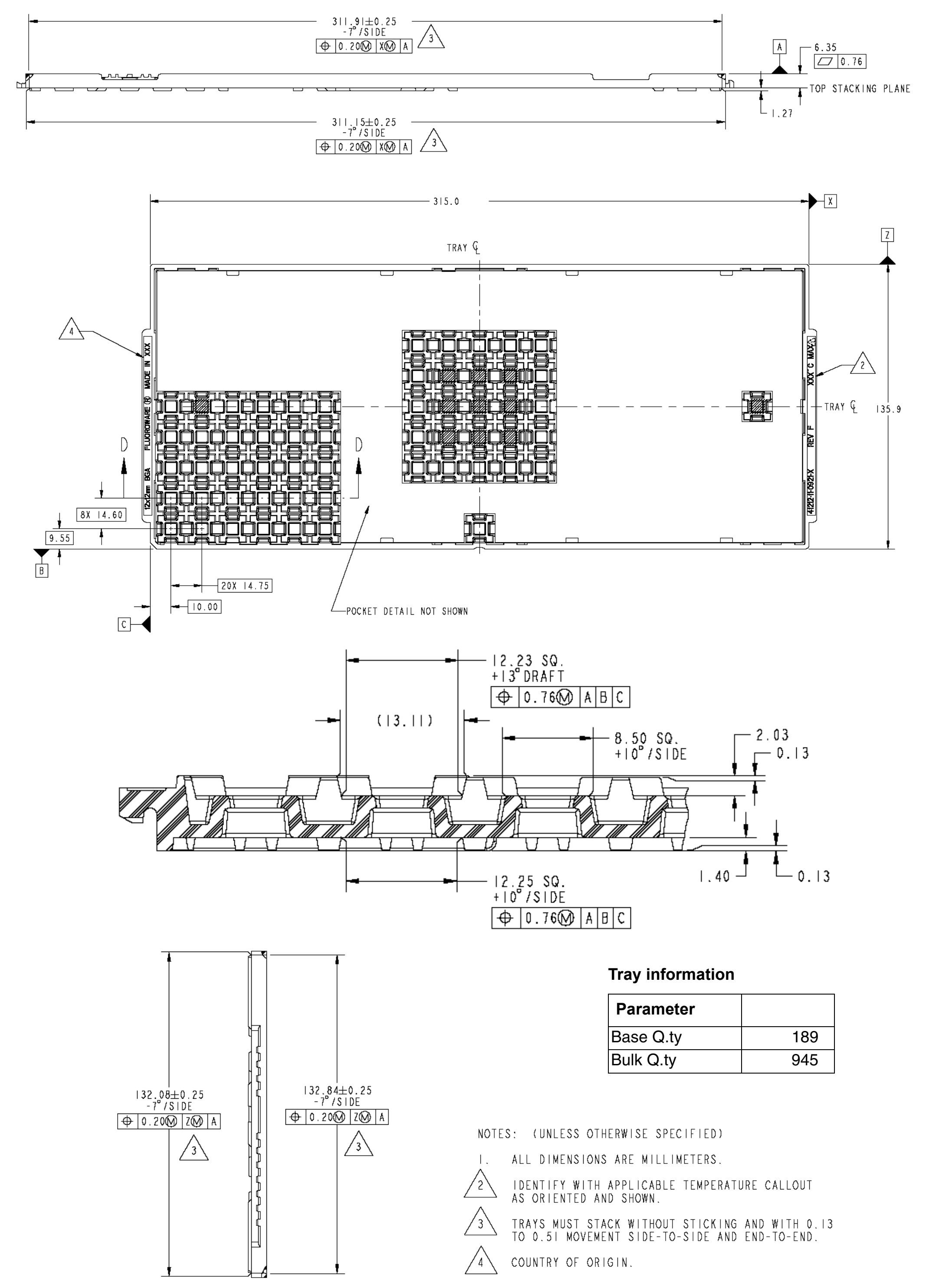
Description	Dimension	mm
Tape width	W	32
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	2
Hole Position	F (± 0.1)	14.2
Compartment Depth	K (max)	2.2



5.5 PQFN - 12x12 power lead-less packing information

The devices can be packed in tray or tape and reel shipments (see *Table 19: Device summary*).

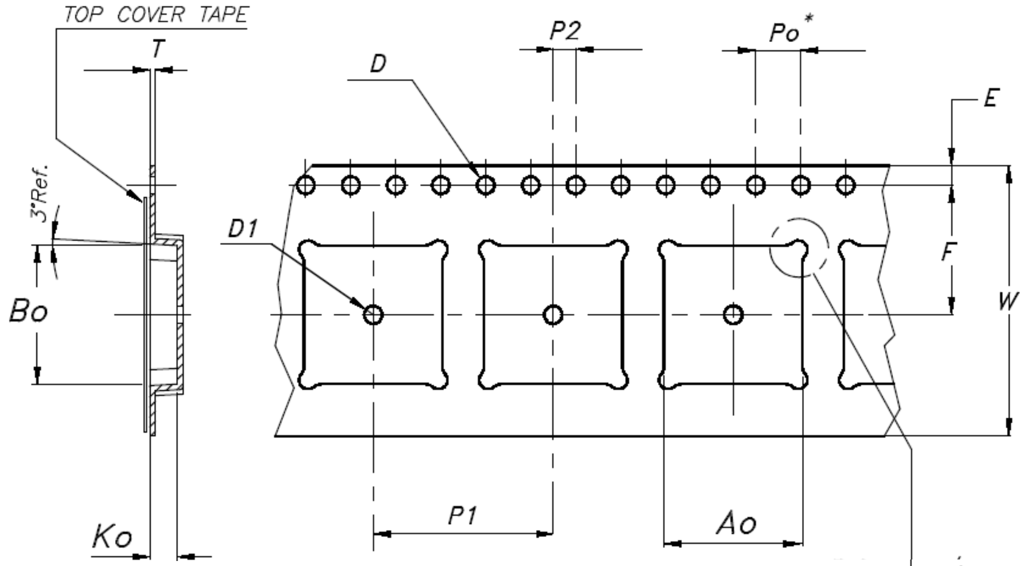
Figure 47. PQFN - 12x12 power lead-less tray shipment (no suffix)

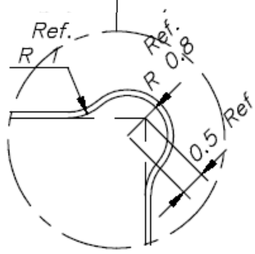


Tray information

Parameter	
Base Q.ty	189
Bulk Q.ty	945

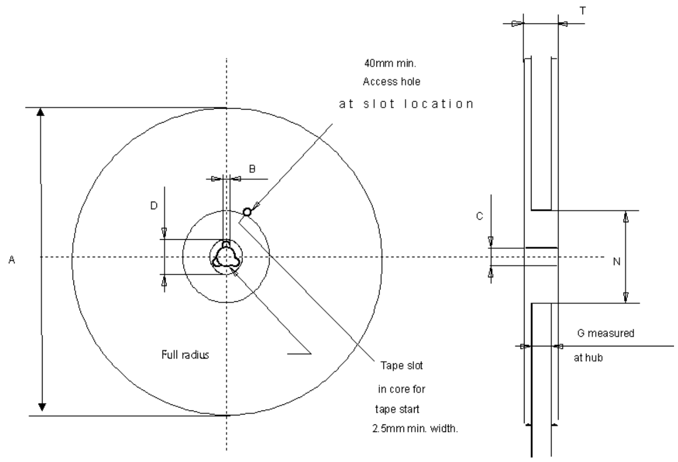
Figure 48. PQFN - 12x12 power lead-less tape and reel shipment (suffix “TR”)





Tape dimensions

Dimension	mm
A0 ± 0.1	12.30
B0 ± 0.1	12.30
K0 ± 0.1	2.15
F ± 0.1	11.50
E ± 0.1	1.75
W ± 0.3	24
P2 ± 0.1	2
P0 ± 0.1	4
P1 ± 0.1	16
T ± 0.05	0.30
D	1.50
D1 (min)	1.50



Reel dimensions

Dimension	mm
Base Q.ty	1500
Bulk Q.ty	1500
A (max)	330
B (min)	1.5
C (± 0.2)	13
D (min)	20.2
G (+ 2 / -0)	32
N (min)	100
T (max)	38.4

6 Order codes

Table 19. Device summary

Package	Order codes		
	Tube	Tape and reel	Tray
PQFN-12x12 power lead-less	—	VND5E004ATR-E	VND5E004A-E
MultiPowerSO-30	VND5E004A30-E	VND5E004A30TR-E	—

7 Revision history

Table 20. Document revision history

Date	Revision	Changes
20-Jul-2010	1	Initial release.